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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,414	12/12/2003	Wen-Fa Sung	AUOP0004USA	1413

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER
ZIMMERMAN, GLENN

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,414	SUNG ET AL.	
	Examiner	Art Unit	
	Glenn Zimmerman	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 December 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 34. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the showing of the electrode pairs are disposed on a bottom surface of the front plate, also a second dielectric layer having a second predefined pattern disposed on a bottom surface of the front plate, a fluorescent layer covering the second dielectric layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: phosphorous layer.

The disclosure is objected to because of the following informalities: In paragraph 14, the examiner suggests changing "Fig. 3is" to - - Fig. 3 is - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Amemiya et al. U.S. Patent 6,492,770 B2.

Regarding claim 1, Amemiya et al. discloses a plasma panel **(title)** comprising:

A rear plate **(back glass substrate Fig. 2 ref. 13)**; a front plate **(front glass substrate ref. 10)** parallel **(col. 3 lines 1-4)** with and spaced apart from the rear plate; a plurality of electrode pairs **(bus electrodes or transparent electrodes refs. Xa and Ya or ref. Xb and Yb)** disposed in parallel **(col. 2 lines 24-25)** with each other; and a first

dielectric layer **(dielectric layer ref. 11; ref. 11 clearly shows a pattern as the layer gets thicker and thinner; also Fig. 18 ref. 21)** having a first predefined pattern covering the electrode pairs.

Regarding claim 2, Amemiya et al. discloses the plasma panel of claim 1 wherein each of the electrode pairs has an equal spacing **(discharge gap Fig. 1 ref. G; discharge space S)**.

Regarding claim 3, Amemiya et al. discloses the plasma panel of claim 1 wherein the electrode pairs are disposed on a bottom surface of the front plate **(bus electrodes or transparent electrodes Fig. 2 refs. Xa and Ya or ref. Xb and Yb)**.

Regarding claim 4, Amemiya et al. discloses the plasma panel of claim 3 further comprising a second dielectric layer **(white dielectric layer Fig. 9 ref. 14)** having a second predefined pattern disposed on a top surface of the rear plate.

Regarding claim 5, Amemiya et al. discloses the plasma panel of claim 4 further comprising a fluorescent layer **(plasma layer ref. 16)** covering the second dielectric layer.

Regarding claim 9, Amemiya et al. discloses the plasma panel of claim 1 wherein a discharge gap is formed between two electrodes **(transparent electrodes Fig. 2 refs. Xb and Yb)** of each of the electrode pairs **(discharge gap Fig. 1 ref. G)**.

Regarding claim 12, Amemiya et al. discloses the plasma panel of claim 1 further comprising a plurality of spacers **(partition walls ref. 35)** disposed between the front plate and the rear plate.

Claims 1 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Moore U.S. Patent 6,570,339.

Regarding claim 1, Moore discloses a plasma panel **(title)** comprising:

A rear plate **(ref. 24)**; a front plate **(ref. 16)** parallel **(Fig. 3, 4; top fiber array)** with and spaced apart from the rear plate; a plurality of electrode pairs **(Fig. 32 ref. 33a and 33b)** disposed in parallel **(Fig. 3; fiber array)** with each other; and a first dielectric layer **(glass fiber structure ref. 37)** having a first predefined pattern covering the electrode pairs **(Fig. 32 shows pattern covering)**.

Regarding claim 6, Moore discloses a plasma panel wherein the electrode pairs are disposed on a top surface of the rear plate **(bottom plate Fig. 4 ref. 24; Fig. 4 ref. 37, 33b, and 33a disposed on ref. 24)**.

Regarding claim 7, Moore discloses the plasma panel of claim 6 further comprising a second dielectric layer **(array of fibers ref. 47)** having a second predefined pattern **(Figure 4 clearly shows a patterned ref. 47)** disposed on a bottom surface of the front plate **(ref. 16 top glass plate)**.

Regarding claim 8, Moore discloses the plasma panel of claim 7 further comprising a fluorescent layer **(phosphors Fig. 8 ref. 23R, 23G and 23B)** covering the second dielectric layer.

Regarding claim 9, Moore discloses the plasma panel of claim 1 wherein a discharge gap is formed between two electrodes of each of the electrode pairs **(Fig. 32 shows the gap between 33a and 33b)**.

Claims 1, 3 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Moore U.S. Patent Application Publication 2001/0033483.

Regarding claim 1, Moore discloses a plasma panel **(title)** comprising:

A rear plate **(inner glass sleeve Fig. 16 ref. 75)**; a front plate **(outer glass sleeve)** parallel **(Fig. 16)** with and spaced apart from the rear plate; a plurality of electrode pairs **(wire electrodes Fig. 16 ref. 11)** disposed in parallel **(Fig. 16, 5)** with each other; and a first dielectric layer **(linear glass structure ref. 27)** having a first predefined pattern covering the electrode pairs **(Figures 1-4 and 16 show the predetermined pattern)**.

Regarding claim 3, Moore discloses the plasma panel of claim 1 wherein the electrode pairs are disposed on a bottom surface of the front plate **(outer side Fig. 17 ref. 75)**.

Regarding claim 10, Moore discloses the plasma panel of claim 1 further comprising a fluorescent layer **(phosphor layer Fig. 4, 16 ref. 23)** covering the first dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore U.S. Patent Application Publication 2001/0033483 in view of Chikazawa U.S. Patent 5,932,967.

Regarding claim 11, Moore teaches all the limitations of claim 11, but fails to teach wherein the fluorescent layer is a phosphorous layer. Chikazawa in the analogous art teaches a phosphorous layer **(ref. 7 col. 2 lines 45 and 46)** . Additionally, Chikazawa teaches incorporation of such a phosphorous layer to improve conversion of UV light into visible rays **(col. 1 lines 45-50)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use phosphorous in the fluorescent/phosphor of Moore, since such a modification would improve conversion of UV light into visible rays as taught by Chikazawa.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Zimmerman whose telephone number is (571) 272-2466. The examiner can normally be reached on M-W 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh D Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn Zimmerman

Vip Patel
Primary Examiner
AU 2879